Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1   1.   (Currently amended): A computing device that provides hardware

2 conversion of control flow ~~to predicates associated with program instructions~~ in machine code

3 that is executable ~~within~~ by said computing device, said machine code also being executable by a

4 target computing device different from said computing device, said computing device

5 comprising:

6   predicate assignment means for detecting the beginning and the end of a branch

7 domain of said ~~program instructions~~ machine code, said predicate assignment means being

8 invisible to instruction set architecture and thereby invisible to a user; and

9   predicate use means for realizing the beginning and the end of said branch domain

10 at execution time, and for selectively enabling and disabling ~~instructions~~ machine code within

11 said branch domain, said predicate use means being invisible to instruction set architecture and

12 thereby invisible to a user~~,~~.

13   wherein said machine code is executable by said computing device without

14 recompiling, so that the same machine code is executable by said target computing device and by

15 said computing device.

1   2.   (Currently amended): The computing device according to claim 1 wherein

2 said predicate assignment means includes a tracking buffer comprising dedicated ~~register~~ storage

3 to store branch information in order to make said predicate assignments.

1   3.   (Previously presented): The computing device according to claim 1,

2 wherein said predicate assignment means is operative to assign a canceling predicate to said

3 branch domain in order to delineate said branch domain so that effects of its corresponding

4 branch are nullified.

Appl. No. 09/838,678
Amdt. dated December 27, 2004
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group

PATENT

1   4.   (Currently amended): The computing device according to claim 3,

2 wherein said predicate use means further includes dedicated registers for ~~each instruction~~said

3 machine code in order to effect arbitrary control flow, said branch domain including at least a

4 disjoint branch domain, a nested branch domain, overlapped branch domains, or a ~~and~~

5 combinations of said branch domains.

1   5.   (Currently amended): A method for providing hardware conversion of

2 control flow to predicates in order to enable ~~program instructions~~ a set of machine code

3 comprising a computer program to be executable within a computing device, said set of machine

4 code being executable within a target computing device different from said computing device,

5 said method comprising:

6   detecting the beginning and the end of a branch domain of selected said ~~program~~

7 ~~instructions~~machine code in a manner that is invisible to instruction set architecture and thereby

8 is invisible to a user;

9   generating from each said branch domain a predicate;

10   associating said predicate with at least one ~~program instruction~~machine code; and

11 thereafter

12   realizing the beginning and the end of said branch domain at execution time

13 thereby selectively enabling and disabling ~~instructions~~ execution of machine code within said

14 branch domain.

1   6.   (Currently amended): The method according to claim 5 wherein said

2 detecting step includes using a tracking buffer to store branch information to make said predicate

3 assignments.

1   7.   (Previously presented): The method according to claim 5 wherein said

2 predicate generating step assigns a canceling predicate to said branch domain in order to

3 delineate said branch domain so that effects of its corresponding branch are nullified.

Appl. No. 09/838,678
Amdt. dated December 27, 2004
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group

PATENT

1   8.   (Currently amended): The method according to claim 7, wherein said

2 predicate generating further includes using dedicated registers for ~~each instruction~~ said machine

3 code in order to effect arbitrary control flow, said branch domain including at least a disjoint

4 branch domain, a nested branch domain, overlapped branched domains, or a ~~and~~ combinations of

5 said branch domains.